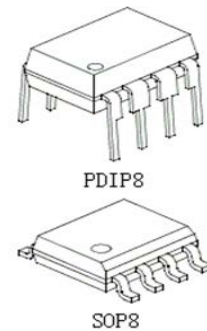


# BL6562 ACTIVE PFC CONTROLLER

## 1 Features

- ◆ Transition-mode control
- ◆ Low start-up current (<70uA)
- ◆ Ultra-low quiescent current  $\leq 2\text{mA}$
- ◆ Ultra-low operating current  $\leq 2.2\text{mA}$
- ◆ Large IC supply voltage operating range
- ◆ Supply current  $\leq 1\text{mA}$  after disable
- ◆ 1%(@ $T_j=25^\circ\text{C}$ ) internal reference voltage
- ◆ System operation protection:
  - Dynamic and static over voltage protection
  - Under-voltage lockout function
  - Peak current limited
  - Supply voltage upper clamped
  - Output voltage upper clamped
- ◆ -400mA/+600mA totem pole output driver with UVLO pull-down



**Figure1 PACKAGES**

## Applications

- ◆ LED Light Driver
- ◆ Electronic Ballast
- ◆ AC/DC Adapter

## 2 General descriptions

BL6562 is an active power factor correct controller operating in transition mode, which is mainly used in small power electronic ballast, LED light driver and AC/DC adapter.

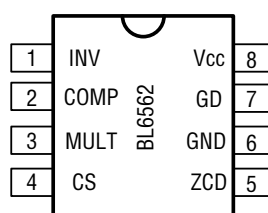
Realised in advanced BCD technology, BL6562 features ultra-low start-up current and operating current ( $\leq 2.2\text{mA}$  @12V). Remote IC DISALBE function can make it work at power saving mode.

BL6562 includes an internal highly linear multiplier, able to provide a high power factor in wide-range-mains operation and over a large range load change. The max current of the MOSFET is limited to the upper clamp output voltage of the multiplier.

Dynamic and static over-voltage protection, internal supply voltage upper clamp、under voltage lockout and output upper clamp functions can make the system work safely.

-400mA/+600mA totem pole output driver is capable of driving large power MOSFET and IGBT.

## Figure 2 Pin connection

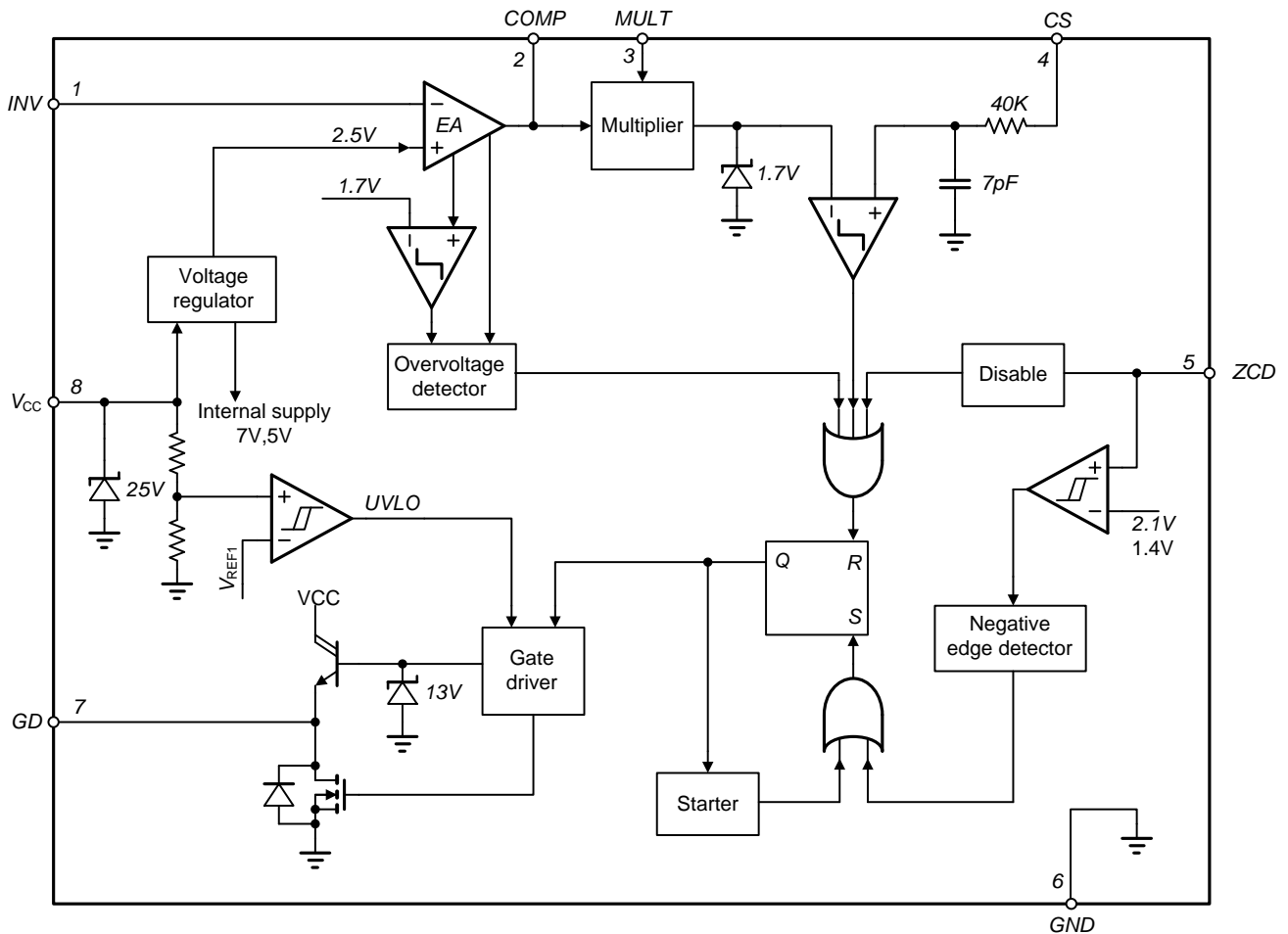


8 LEAD SOP or DIP

**Table 1 Pin description**

Pin	Symbol	Function description
1	INV	Inverting input of the error amplifier.
2	COMP	Output of the error amplifier and one input of the multiplier.
3	MULT	One input of the multiplier.
4	CS	One input of Current sense comparator. An internal low pass filter is placed to reduce high frequency interface.
5	ZCD	Zero current detection input and disable function pin. When the voltage is smaller than 130mV, the device is disabled.
6	GND	Ground.
7	GD	Gate driver output. The typical upper output clamp voltage is 12V.
8	Vcc	Supply input. Supply voltage of UVLO block, voltage regulator and output driver. The upper limit is extended to 24V min.

**Figure 3 Block diagram**





**Table 2 Absolute maximum ratings**

Parameter	symbol	Value	Unit
Supply voltage	$V_{CC}$	24.5	V
inputs and outputs voltages(Pin1~4)		-0.3~8	V
Zero current detector current	$I_{ZCD}$	+/-10	mA
Gate driver output voltage	$V_{GD}$	-0.3~self-limited	
Power dissipation@50°C(DIP-8)	$P_{total}$	1	W
Power dissipation@50°C(SO-8)	$P_{total}$	0.65	W
Junction temperature operating range	$T_j$	-40~150	°C
Storage temperature	$T_{stg}$	-55~150	°C
ESD(HBM) voltage	$V_{ESD}$	>4000	V
Latch up current	$I_{Latchup}$	>200	mA

**Table3 Electrical characteristics**

( $T=25^{\circ}C$ ,  $V_{CC}=12V$ ,  $C_O=1nF$ ; unless otherwise specified)

symbol	parameter	Test condition	min	typ	max	unit
<b>Supply block</b>						
$V_{CC-on}$	Turn-on threshold		11	12	13	V
$V_{CC-off}$	Turn-off threshold		9	9.5	10.2	V
$V_{CC}$	Operating rang	After turn-on	10.3		24	V
$V_{CC,clamp}$	Upper clamp voltage	$I_{CC}=20mA$	24.5	25.8	28	V
$V_{R25}$	2.5V reference voltage	$T=25^{\circ}C$	2.475	2.5	2.525	V
		$10.3V < V_{CC} < 24$	2.45		2.55	
<b>Supply current</b>						
$I_{st}$	Start-up current	$V_{CC}=11V$ before turn on		40	70	uA
$I_q$	Quiescent current			1.3	2	mA
$I_{CC}$	Operating current	@70kHz		1.5	2.2	mA
$I_{qsdisc}$	Quiescent current when DISABLE	$V_{zcd}=120mV$		0.67	1	mA
$I_{qsovp}$	Quiescent current when OVP	OVP		1.3	2	mA
<b>Multiplier block</b>						
$I_{mul}$	Input bias current	$V_{mult}=4V$			-1	uA
$L_{mul}$	Linear operating range		0~3			V
$k_{max}$	Max slope	$V_{mult}=0\sim0.5V$ , $V_{comp}=5.2V$	1.6	1.9		V/V
K	Gain(1)	$V_{mult}=1V, V_{comp}=4V$	0.5	0.6	0.7	1/V
$V_{multoffset}$	Multiplier offset	$V_{mult}=0V$		27		mV
		$V_{mult}=2.5V$		5		mV
$V_{multclamp}$	Output clamp voltage	$V_{comp}=5.2V$	1.6	1.7	1.8	V

**Table 3 Electrical characteristics (continued)**(T=25°C, V<sub>cc</sub>=12V, C<sub>0</sub>=1nF; unless otherwise specified)

Error amplifier block						
I <sub>inv</sub>	Input bias current	V <sub>inv</sub> = 3V			-1	uA
A <sub>v</sub>	Open loop voltage gain		60	80		dB
GBW	Gain Bandwidth			1		MHz
I <sub>comp</sub>	Source current	V <sub>comp</sub> =4V, V <sub>inv</sub> =2.4V	-2	-3.5	-5	mA
	Sink current	V <sub>comp</sub> =4V, V <sub>inv</sub> =2.6V	4	6		mA
V <sub>comp</sub>	upper clamp voltage	I <sub>source</sub> =-0.5mA	5.2	5.35	5.8	V
	Lower clamp voltage	I <sub>sink</sub> =0.5mA	0.8	1	1.2	V
Over voltage protector						
I <sub>ovp</sub>	Dynamic OVP threshold current		24	39	45	uA
Hys		(2)		20		uA
V <sub>ovp</sub>	Static OVP threshold voltage	(2)	1.6	1.7	1.8	V
Current sense block						
I <sub>cs</sub>	Input bias current	V <sub>cs</sub> =0			-1	uA
t <sub>d(H-L)</sub>	Delay to output			250	350	ns
Zero current detector block						
V <sub>zcd(H)</sub>	Upper clamp voltage	I <sub>zcd</sub> =2.5mA	5	5.8	6.5	V
V <sub>zcd(L)</sub>	Lower clamp voltage	I <sub>zcd</sub> =-2.5mA	0.3	0.55	0.8	V
I <sub>zcdb</sub>	Input bias current	V <sub>zcd</sub> =1 to 4.5V		2		uA
V <sub>ZCDA</sub>	Positive triggering voltage	(2)		2.1		V
V <sub>ZCDT</sub>	Negative triggering voltage	(2)		1.4		V
I <sub>zcdsor</sub>	Source current capability		-2.5		-5.5	mA
I <sub>zcdsink</sub>	Sink current capability		2.5			mA
V <sub>zcd dis</sub>	Disable threshold		130	160	190	mV
V <sub>zcd en</sub>	Enable threshold		250	280	310	mV
I <sub>zcdres</sub>	Restart current		40	80		uA
Starter block						
f <sub>start</sub>	Starter frequency		5	9	16	KHz
Output gate driver block						
V <sub>oh</sub>	Output voltage	I <sub>GDsource</sub> =20mA	9.8	10.3		V
		I <sub>GDsource</sub> =200mA	8	8.3		V
V <sub>ol</sub>		I <sub>GDsink</sub> =200mA		1	1.9	V
t <sub>f</sub>	Fall time			32	70	ns
t <sub>r</sub>	Rise time			45	85	ns
V <sub>oclamp</sub>	Output clamp voltage	V <sub>cc</sub> =20V, I <sub>GDsource</sub> =5mA	11	12	13	V
V <sub>o-uvlo</sub>	Output voltage before turn on	V <sub>cc</sub> =0~V <sub>CCon</sub> , I <sub>GDsink</sub> =10mA			1	V

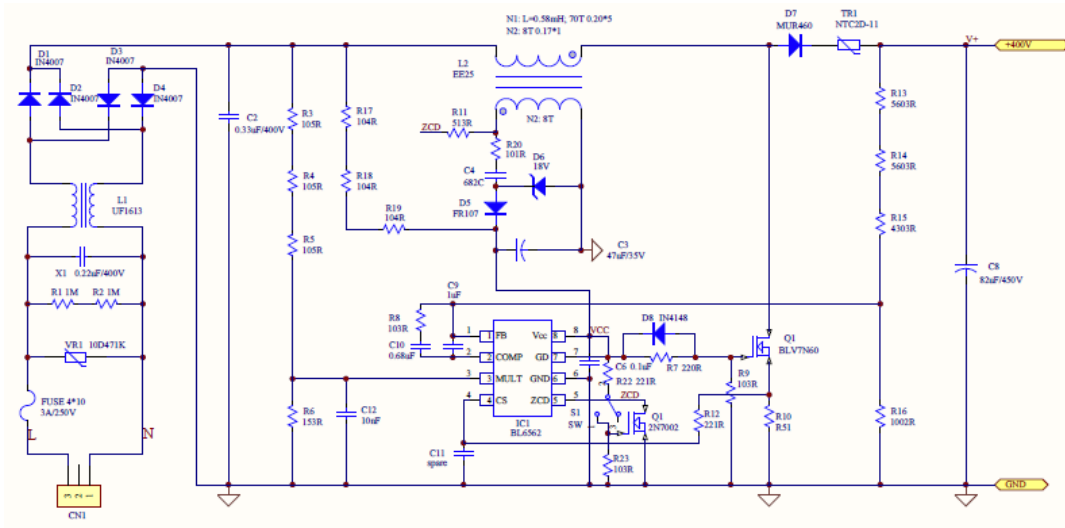
(1) K= V<sub>CS</sub>/ [V<sub>mult</sub>\*(V<sub>comp</sub>-2.5)]

(2)Parameters guaranteed by design.

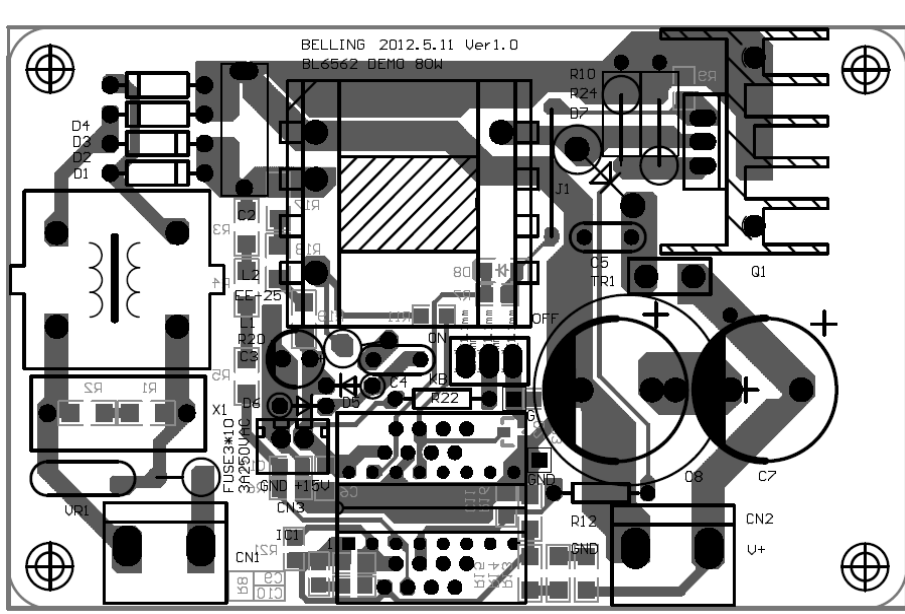


### 3 Application information

**Figure 4 Wide-range mains demo board BL6562-80W: schematic**



**Figure 5 Wide-range mains demo board BL6562-80W: PCB layout**



**Table 4 BL6562-80W test results**

V <sub>in</sub> (V <sub>AC</sub> )	P <sub>in</sub> (W)	V <sub>o</sub> (V <sub>DC</sub> )	ΔV <sub>o</sub> (V <sub>pp</sub> )	P <sub>o</sub> (W)	η (%)	PF	THD(%)
85	86.6	391.75	15	80.19	92.6	0.998	3.4
110	84.7	391.83	15	80.21	94.7	0.998	4.6
135	83.8	391.83	15	80.21	95.7	0.997	5.4
175	83.2	391.85	15	80.21	96.4	0.997	5.8
220	82.9	391.87	15	80.21	96.8	0.991	6.7
265	82.7	391.87	15	80.21	97.0	0.978	8.2



## 4 Package information

Figure 6 DIP8 package dimensions

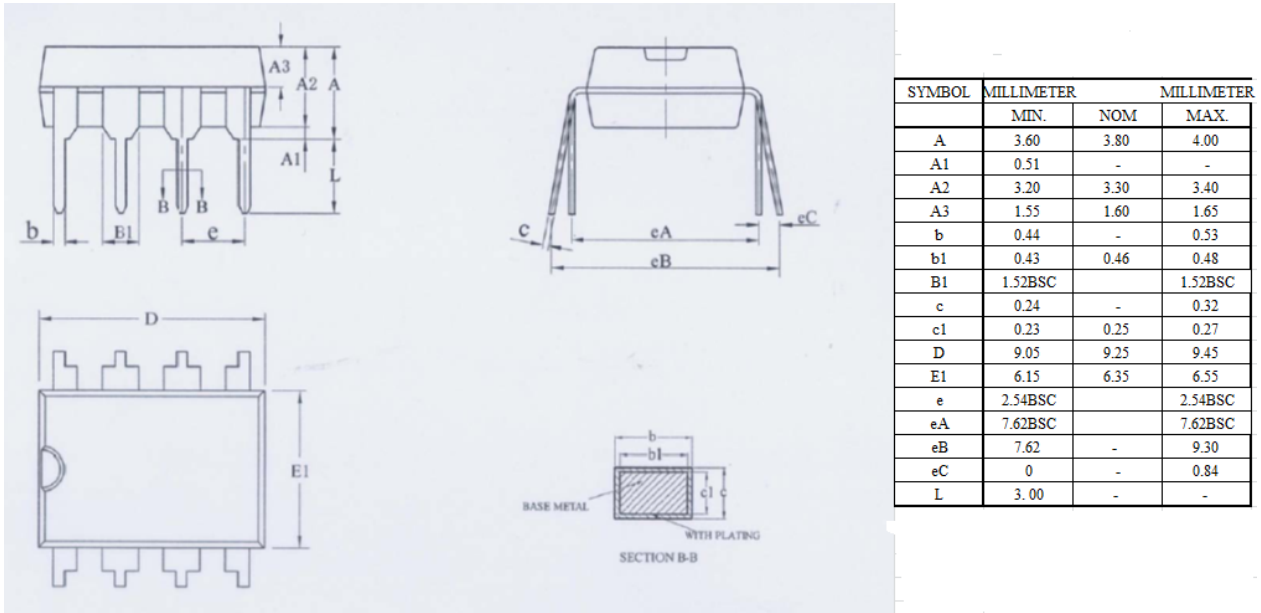
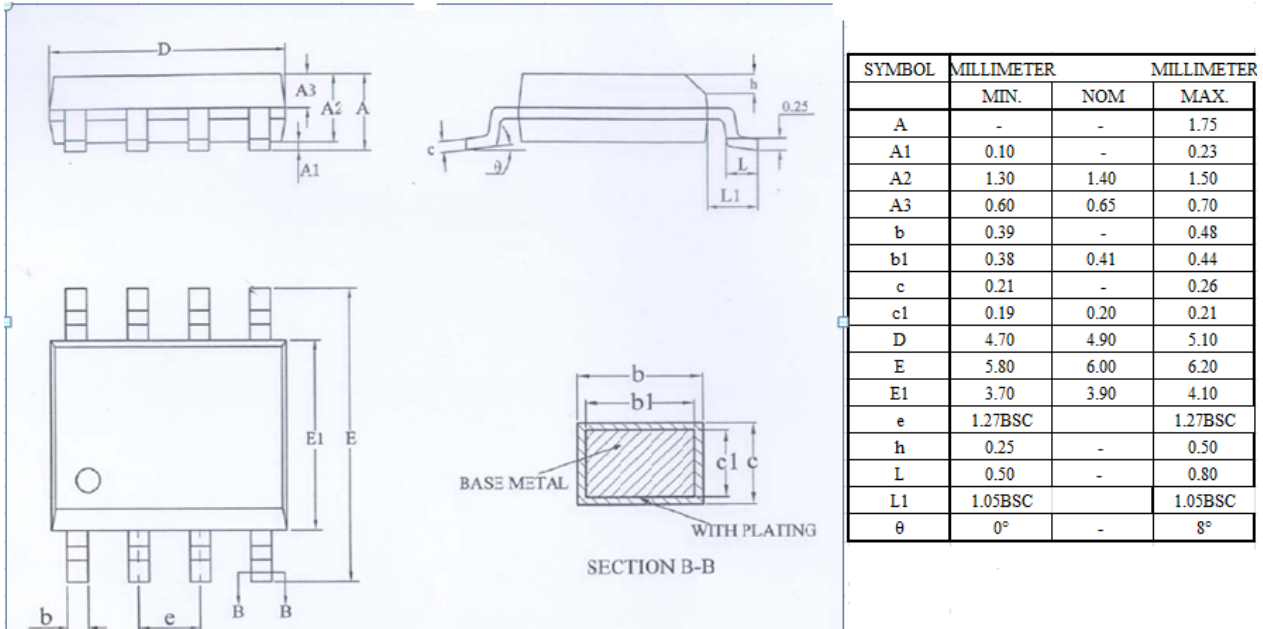


Figure 7 SOP8 package dimensions



Notice: Sample tested during initial release and after any redesign or process change that may affect parameter. Specification subject to change without notice. Please ask for the newest product specification at any moment.